IN THE CLAIMS:

Listing of claims:

1-5. (canceled)

6. (previously presented) A method for manufacturing a semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi-recessed LOCOS layer is to be formed;

implanting an impurity in a semiconductor substrate in the first recessed section and in the second recessed section; and

thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section.

7. (original) A method for manufacturing a semiconductor device according to claim 6, further comprising forming an anti-oxidation layer having a predetermined pattern, wherein the thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section is conducted using the anti-oxidation layer formed on the semiconductor substrate as a mask.

8. (original) A method for manufacturing a semiconductor device according to claim 7, wherein the anti-oxidation layer has a film thickness of 50 – 70 nm.

9. (previously presented) A method for manufacturing a semiconductor device according to claim 7, wherein the substrate includes side surfaces and a bottom surface in each of the first recessed section and the second recessed section and further comprising;

before the implanting an impurity, forming a protection film to cover the side surfaces and the bottom surface of semiconductor substrate in the first recessed section and in the second recessed section; and

wherein the implanting includes implanting through the side surfaces and the bottom surfaces.

10. (original) A method for manufacturing a semiconductor device according to claim 9, wherein the protection film is a silicon oxide layer.

11. (original) A method for manufacturing a semiconductor device according to claim 10, wherein the silicon oxide layer is formed by a thermal oxidation method.

12. (original) A method for manufacturing a semiconductor device according to claim 9, further comprising, after the implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section, removing the protection film.

13. (original) A method for manufacturing a semiconductor device according to claim 6, wherein the first recessed section and the second recessed section each are formed in a tapered configuration.

14. (previously presented) A method for manufacturing a semiconductor device according to claim 13, wherein a tapered angle of each of the first recessed section and the second recessed section is 60 degrees or greater and less than 90 degrees.

15. (original) A method for manufacturing a semiconductor device according to claim 6, wherein an implanting direction of the impurity traverses a normal line of a surface of the semiconductor substrate during the implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section.

16. (previously presented) A method for manufacturing a semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi-recessed LOCOS layer is to be formed;

implanting an impurity in a semiconductor substrate in the first recessed section and in the second recessed section; and

thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section;

wherein the implanting direction of the impurity and the normal line of the surface of the semiconductor substrate during the implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section defines an angle that is greater than zero degrees and no greater than 45 degrees.

17-20. (canceled)

21. (previously presented) A method for manufacturing a semiconductor device including a semiconductor substrate, the semiconductor device comprising first and second field effect transistors and an element isolation region between the first and second field effect transistors, the first and second field effect transistors each including: (a) a gate dielectric layer, (b) a source region, (c) a drain region, (d) a first semi-recessed LOCOS layer provided between the gate dielectric layer and the drain region, (e) a second semi-recessed LOCOS layer provided between the gate dielectric layer and the source region, (f) a first offset impurity layer provided below the first semi-recessed LOCOS layer, and (g) a second offset impurity layer provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in regions where the first semi-recessed LOCOS layer is to be formed, a second recessed section in regions where the second semi-recessed LOCOS layer is to be formed and a third recessed section in a region where the element isolation region is to be formed;

implanting an impurity in the semiconductor substrate in the first and second recessed sections and in part of the third recessed section;

heating the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section, the second semi-recessed LOCOS layer in the second recessed section, and a third semi-recessed LOCOS layer in the third recessed section;

wherein the first semi-recessed LOCOS layer is positioned between and in contact with the source region and the gate dielectric region, and the second semi-recessed LOCOS layer is positioned between and in contact with the drain region and the gate dielectric region; and

wherein the implanting is controlled so that the first and second offset impurity layers are formed to each include a side portion that extends along a lower surface of the gate dielectric region.

22. (previously presented) A method for manufacturing a semiconductor device as in claim 21, further comprising forming a channel stopper layer by implanting an impurity below a central portion of the element isolation region; and forming low concentration impurity layers below end portions of the element isolation region; wherein the channel stopper layer is formed to be spaced apart from the low concentration impurity layers.

23. (previously presented) A method for manufacturing a semiconductor device as in claim 22, further comprising forming an anti-oxidation layer having a predetermined pattern on the semiconductor substrate, wherein the thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section is conducted using the anti-oxidation layer formed on the semiconductor substrate as a mask.

24. (previously presented) A method for manufacturing a semiconductor device according to claim 21, where the first recessed section, the second recessed section and third recessed section of the substrate each include side and bottom surfaces, the method further comprising:

before the implanting, forming a protection film covering the side and bottom surfaces of the first recessed section, the second recessed section and the third recessed section; and

wherein the implanting an impurity in the semiconductor substrate in the first and second recessed sections and in part of the third recessed section includes implanting through the side surfaces and the bottom surfaces of the first and second recessed sections and through the side surfaces and part of the bottom surface of the third recessed section.

25. (previously presented) A method for manufacturing a semiconductor device according to claim 24, further comprising forming the side surfaces of the first, second and third recessed sections to be tapered inward towards the bottom surface, so that a width of the recessed sections is smaller at the bottom surface than at a distance above the bottom surface.

26. (previously presented) A method for manufacturing a semiconductor device according to claim 25, wherein the taper angle is in the range of 100 to 110 degrees at the intersection of the side surfaces with the bottom surface.

27. (previously presented) A method for manufacturing a semiconductor device including a semiconductor substrate, the semiconductor device comprising first and second field effect transistors and an element isolation region between the first and second field effect transistors, the first and second field effect transistors each including: (a) a gate dielectric layer, (b) a source region, (c) a drain region, (d) a first semi-recessed LOCOS layer provided between the gate dielectric layer and the drain region, (e) a second semi-recessed LOCOS layer provided between the gate dielectric layer and the source region, (f) a first offset impurity layer provided below the first semi-recessed LOCOS layer, and (g) a second offset impurity layer provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in regions where the first semi-recessed LOCOS layer is to be formed, a second recessed section in regions where the second semi-recessed LOCOS layer is to be formed and a third recessed section in a region where the element isolation region is to be formed;

performing a first implantation to implant ions into the semiconductor substrate in the first and second recessed sections and in end regions of the third recessed section;

performing a second implantation to implant ions into the substrate at a central region of third recessed section;

heating the semiconductor substrate in an atmosphere containing oxygen to form the first semi-recessed LOCOS layer in the first recessed section, the second semi-recessed LOCOS layer in the second recessed section, and a third semi-recessed LOCOS layer in the third recessed section;

wherein the heating is also used to also diffuse the first implantation ions into the substrate and form the first and second offset impurity layers in the first and second field effect transistors and form low concentration impurity layers below the end regions of the third recessed section; and

wherein the heating is also used to diffuse the second implantation ions into the substrate to form a channel stopper layer below the central region of the third recessed section, wherein the channel stopper layer is spaced apart from the low concentration impurity layers.

28. (previously presented) A method for manufacturing a semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising:

forming a silicon oxide nitride layer on a silicon substrate;

forming a silicon nitride layer on the silicon oxide nitride layer;

forming a first recessed section in the substrate where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in the substrate where the second semi-recessed LOCOS layer is to be formed;

implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section; and

thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section, wherein the portions of the substrate having the silicon oxide nitride layer and the silicon nitride layer thereon are not oxidized.

29. (previously presented) A method according to claim 28, wherein the first and second recessed sections each include sidewalls and a lower surface, the method further comprising forming a protective layer covering the sidewalls and the lower surface of the substrate in the first and second recessed sections prior to the implanting an impurity.

30. (previously presented) A method according to claim 6, wherein the first semi-recessed LOCOS layer is positioned between and in contact with the source region and the gate dielectric layer, and the second semi-recessed LOCOS layer is positioned between and in contact with the drain region and the gate dielectric layer, and wherein the implanting is controlled so that the first and second offset impurity layers are formed to each include a side portion that extends along a lower surface of the gate dielectric layer.

31. (previously presented) A method according to claim 6, further comprising forming a gate electrode on the gate dielectric layer, and positioning the gate electrode so that the first semi-recessed LOCOS layer is in contact with the gate dielectric layer under the gate electrode layer and the second semi-recessed LOCOS layer is in contact with the gate dielectric layer under the gate electrode.